Datasheet (DSH)

ZW0102 Z-Wave Single Chip

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REVISION RECORD

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01.01	20020920	TJC	ALL	Initial Issue
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01.03	20041021	TJC	1,2,4,5,8,12,18,22	P 1 : Reference updated to : Z-Wave ZW0102 Application Programming Guide Flash memory : Available code space not listed Interrupt sources bullet updated: 11 Interrupt Sources (5 reserved by Z-Wave API library) Removed : based on preproduction product P 2 : Added : Equinox PPM3 Programmer, ALL-11 Series Programmer Hi-Lo P 4 : Added : Synopsys DW8051 Added : The lock bits can only be set by erasing the whole flash memory P 5 : Added : Note: The SPI is not available in some Z-Wave API libraries P 8 : It is empasized that if POR is disabled then an external power-on-reset / brown-out is required. P 12 : Added : Note: The SPI is not available in some Z-Wave API libraries P 18 : Scenario 1 Note: Added text: Also denoted STOP Mode Scenario 2 Note: Added text: Also denoted Sleep Mode with RTC. Scenario 2 Note: Added text: The chip runs on the RTC clock P 22 : Timing requirement added on RESET_N : rise/fall time must not exceed 400 us.

Table of Contents

1 ABBREVIATIONS

ADC	Analogue to Digital Converter
API	Application Programming Interface
BSIZE	Boot Sector Size
BOBLOCK	Boot Block Lock
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CS	Chip Select
DMA	Direct Memory Access
ESD	Electrical Static Discharge
ESR	Electrical Serial Resistance
FSK	Frequency Shift Keying
GND	Ground
GPIO	General Purpose I/O's
HW	Hardware
I^2C	Inter-Integrated Circuit (Philips' 2-wire serial bus)
LO	Local Oscillator
LSB	Least Significant Byte
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Byte
PCB	Printed Circuit Board
POR	Power-On Reset
PWM	Pulse Width Modulator
RF	Radio Frequency
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SFR	Special Functions Register (8051 processor control registers)
SCK	Serial ClocK
SMD	Surface Mounted Devices
SPI	Serial Peripheral Interface (3-4 wire serial interface)
SPIRE	SPI Read Flash Enable
SRAM	Static Random Access Memory
SW	Software
TBC	To Be Confirmed
TBD	To Be Defined
T/R	Transmit / Receive
UART	Universal Asynchronous Receive Transmit (Asynchronous serial interface)
VCO	Voltage Control Oscillator
ZEROX	Zero crossing

2 INTRODUCTION

2.1 Purpose

The objective of this document is to give a detailed HW datasheet of the Zensys **ZW0102** Z-Wave Single Chip. The document does not include matters pertaining to SW.

2.2 Audience and prerequisites

The target audience of this document is the PCB board designer. No prerequisites are required.

2.3 Datasheet

The datasheet is given on the following pages (1-25).

ZW0102
Z-Wave Single Chip

52 Pins Low Power Z-Wave Transceiver with Microcontroller

SUMMARY

Z-Wave Single Chip

- ***RF Transceiver***
- ***Optimized 8051-Compatible Micro-controller***
- ***Flash Memory for Application and Z-Wave API. Optional Read Back Protection***
- ***2 kbytes SRAM. 128 bytes Micro Controller SRAM***
- ***Triac Controller***
- ***10-bit ADC***
- ***Power-On Reset / Brown-out Detector***
- ***Integrated I/O Peripherals: SPI, UART, PWM output, Flash interface***
- ***3.3 V CMOS***

GENERAL DESCRIPTION

The **ZW0102** Z-Wave Single Chip is a complete wireless solution for home automation consisting of an integrated RF transceiver, an 8051 microcontroller, a Z-Wave SW Application Programming Interface (API) and flash memory storage for user application SW. All of the above is integrated into one single chip. Moreover the **ZW0102** contains a 10-bit ADC, several general purpose I/O pins, a Power-On-Reset circuit / Brown-out detector, a Triac Controller, a Serial Peripheral Interface (SPI), an Interrupt Controller and an UART for connecting to peripheral devices. The chip is designed for very low power and low voltage applications.

The Z-Wave API is described in a separate document: Z-Wave ZW0102 Application Programming Guide.

FEATURES

RF Transceiver
- Freq.: 868.42 (EU) / 908.42 (US) MHz
- High Sensitivity (typical -98 dBm)
- Very low Current Consumption
- Requires very few External Components
- Programmable Output Power typically –29 to 5 dBm
- FSK Modulation
- HW Manchester Encoding/Decoding
- 9.6 kbit/s Data Rate
- Complies with EN 300 220 and FCC CFR47 part 15

8051-Compatible Microcontroller
- Optimized 8051 CPU Core. Typically 3x the performance of a “standard” 8051
- 11 Interrupt Sources (5 reserved by Z-Wave API library)

Memory
- 32 kbyte Flash for Z-Wave API library + Customer Application SW
- R/W/E Access to Flash from CPU
- Read-back Protection of Flash
- 2 kbyte SRAM
- 128 byte CPU dedicated SRAM

Interfaces
- 11 Configurable General Purpose I/O pins
- One High Drive Pin ± 8mA (e.g. for Triac Controller App.)
- One Schmitt Trigger Input (e.g. for Zero Crossing Detection in Triac Controller App.)
- One Input Pin for External Interrupts

Timers

- Timers for Z-Wave SW API + Application SW
  - Two 8051 Compatible Timers
  - Two 16-bit Special Purpose Timers (One is Programmable for PWM).

Up to 115k baud UART

- Debugging via UART

Two Clock Inputs

- Primary clock and RTC clock

External Interrupts

- Level / edge triggered

Triac Controller

10 Bit ADC

- Two Multiplexed Inputs
- V_{DD} or Internal 1.25V Reference
- Max. Sampling Rate 20.96 kHz

Serial Peripheral Interface (SPI)

- Slave in Programming Mode of Internal Flash
- Generic Master for Controlling External SPI Devices (and I^2C devices)

Power-On Reset (POR) / Brown-Out Detector

Power Management

- CPU Power Saving Modes: IDLE and STOP
- System Clock programmable to Primary Clock or RTC
- Power down of ADC, Flash and POR

Power Consumption (typical values)

- Lowest power state: 0.15 µA (must be reset to wake up, POR disabled)
- Low power state: 30 µA (wake up by interrupt, flash disabled))
- CPU only: 9.6 mA
- Receiving: 21 mA
- Transmitting -5dBm: 25 mA
- Transmitting Max (typical +5dBm): 35 mA

Development Tools

The user application SW can be compiled using a standard C-compiler from Keil Software. Please refer to the Keil homepage for Embedded Development Tools (www.keil.com). The **ZW0102** can be programmed using an Equinox EPSILON 5 II programmer, an Equinox PPM3 Programmer or an ALL-11 Series Programmer from Hi-Lo Systems.

ARCHITECTURAL OVERVIEW

Figure 1 shows a functional block diagram of the **ZW0102** architecture.

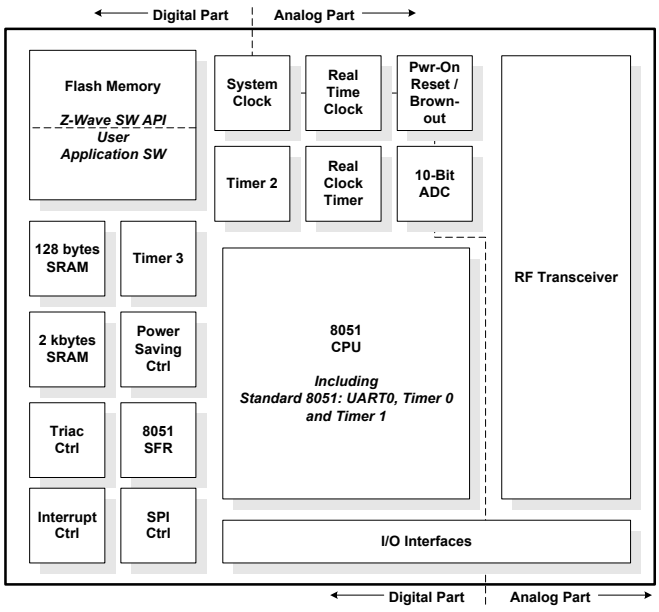


Figure 1: ZW0102 Functional Block Diagram

The central parts of the **ZW0102** are the RF transceiver, the 8051 CPU including SRAM, and the flash memory. In addition to the central parts there are a number of peripheral functions supporting the Z-Wave system. All functional blocks are briefly described below:

Primary Clock

The Primary Clock is the main clock oscillator of the system. The crystal for the system clock must be chosen to 7.376974 MHz with a tolerance of 25 ppm including temperature and ageing.

By default the entire **ZW0102** will run on the Primary Clock. However, it is possible to run the chip on an alternative slower clock (see below). It is also possible to shut down the Primary Clock entirely to reduce power consumption.

Real Time Clock (RTC)

The purpose of the RTC is to provide a real time clock for the RTC timer function. However, the RTC can also be programmed to clock the entire system in order to minimise power consumption. When using the RTC as system clock the RF part will be disabled and it will not be possible to write to the flash.

The RTC is optional in the Z-Wave system. The RTC crystal must to be chosen to 32.768 kHz with an accuracy depending on the application.

After reset the RTC clock is shut down. SW must actively turn it on.

Power-On-Reset / Brown-out Circuit

The Power-On-Reset (POR) circuit eliminates the need for external reset circuitry as it holds the **ZW0102** in reset during power-on and brown-out situations. The POR is designed with glitch immunity and hysteresis for noise and transient stability.

The POR module can be externally disabled (e.g. for power saving). An external power up / brown-out reset must then be provided to the chip using the *RESET_N* pin.

RF Transceiver

The transceiver is able to transmit and receive Z-Wave frames. The transceiver handles all the RF related functions needed for the Z-Wave protocol including Manchester encoding / decoding, pre-ample detection and serialization / deserialization. The high degree of automation in the transceiver minimises the CPU workload.

The RF transceiver needs very few external passive components for input/output matching and VCO. The only part of the VCO that is external is the VCO inductor for tuning the frequency.

It is possible through SW to adjust the output power level or to shut down the RF transceiver completely (in order to reduce power consumption).

A block diagram of the RF transceiver is given in Figure 2.

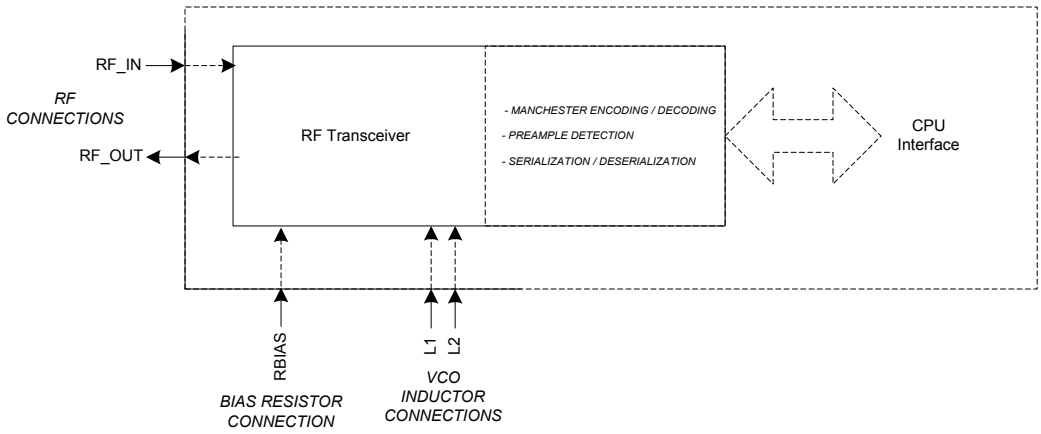


Figure 2: RF Transceiver Architecture

8051 CPU including UART0, Timer 0 & 1

The **ZW0102** contains an embedded 8051 CPU core (Synopsys DW8051) including one standard 8051 serial port and two standard 8051 timers/counters.

The CPU is fully binary compatible with the industry standard 803x/805x micro controllers.

The CPU completes one instruction cycle per four clock cycles.

SFR

The SFR contains the 8051 Special Function Registers that are used to control the operating mode of the 8051 and the built-in peripherals. The registers needed in a given application are operated through the API.

32 Kbytes Flash Memory

The Flash Memory is the CPU program memory containing the Z-Wave API and the application SW. [1] The CPU also has the ability to read, write and erase the Flash. The CPU must run on the primary clock oscillator at times of writing data to the flash.

The **ZW0102** has a built-in read back protection in order to prevent reverse engineering or design theft. Clearing a dedicated lock bit in the flash activates the read back protection. As long as the lock bit is low it is not possible to read from the flash externally (SPI). Other lock bits can protect parts of the flash against writing. The lock bits can only be set high by erasing the whole flash memory.

The Flash Memory can endure at least 20.000 program/erase (P/E) cycles. The flash can be shut down between instruction fetching in order to reduce power consumption. However, this feature should not be used during RF activity, as it will affect the RF performance.

The Flash Memory is accessed and programmed through the SPI serial interface.

[1] External code memory signals as in standard 8051's are not supported due to the limited number of pins.

128 bytes SRAM

This built-in SRAM is used by the CPU as internal register memory. The RAM may also be accessed through direct instructions from the CPU.

2 kbytes SRAM

The built-in 2kbytes SRAM are used by the CPU as "8051 external data" memory

RTC Timer

The RTC Timer is a programmable real clock timer that can be programmed to generate periodical interrupts for the system. The Timer runs on the RTC.

Timer 2 and 3

Timers 2 and 3 are versatile timers that can be polled or programmed to generate interrupts. Each interrupt timer uses a configurable auto-reload counter with a fixed clock divider (clock is divided by 255).

Timer 2 can also be set in PWM (Pulse Width Modulation) mode with the output on the *P34/PWM2/T0* pin. The PWM has a configurable 8 bit prescaler and a configurable duty cycle. Figure 3 shows the timing of a PWM output:

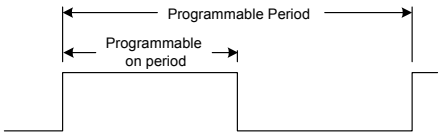


Figure 3: PWM Output

Interrupt Controller

The Interrupt Controller controls the interrupt priority assignment. The microcontroller supports 12 interrupt sources. One external interrupt is supported using a dual function General Purpose I/O.

Triac Controller

The **ZW0102** contains a triac controller for power regulating applications. Using an external triac and a few extra external passive components, a complete phase control circuit can be designed. The function is mostly implemented in HW in order to minimise CPU workload. The controller generates triac fire pulses using 1) the time of zero crossing of the AC mains measured on the pin *ZEROX* and 2) a dimming level set by SW.

10 bit ADC

A 10bit ADC that can be programmed to refer to V_{DD} or an internal voltage reference. The ADC has two multiplexed analogue inputs.

The ADC features a number of different modes for single- and multi-conversion. It has a built-in comparator for generating interrupts or system reset when a certain programmed threshold is exceeded.

Furthermore it is possible to have the ADC running while the CPU and built-in peripherals are in IDLE or STOP mode. In this case it can be programmed to wake up the processor when the comparator condition holds true.

It is possible to shut down the ADC for reducing power consumption.

Serial Peripheral Interface - SPI

The SPI has two purposes: 1) to provide external access to the Flash memory and 2) to allow **ZW0102** to communicate with peripheral devices such as external EEPROM[2]. *Note: The SPI is not available for customer application in some Z-Wave API libraries.*

The **ZW0102** is SPI master during normal operation. It is only a slave during Flash programming where an external SPI master must control the bus.

[2] Note: SPI devices cannot be mapped into the CPU's memory space!

Power Control

The Power Control Block controls the chip's different power saving modes. The **ZW0102** supports numerous power saving modes as listed below:

- Two power saving modes for CPU: IDLE and STOP. IDLE halts the CPU but leaves CPU peripherals and internal clocks active. In STOP mode, the CPU is halted, and all memories and logic except for ADC are rendered inactive.
- Disabling the Flash (when CPU is in IDLE) or configure it for power down between each read access. The latter should not be used in conjunction with RF receptions or transmissions, as it will degrade the RF performance.
- Disabling the POR circuit.
- Disabling the ADC.
- Setting CPU and peripherals to run on RTC (The RF part will be in power down and writing to the flash is disabled)

A simplified block diagram of the clock distribution is given below.

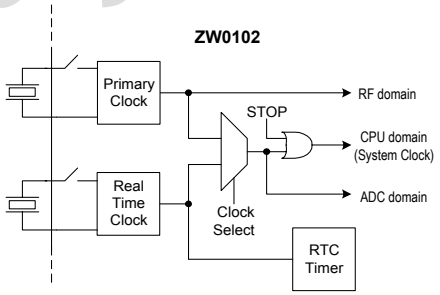


Figure 4: Simplified clock distribution

After power-on all RF and logic modules will run on the primary oscillator and the RTC will be in power down.

When the CPU has entered IDLE mode there are 3 ways to exit the mode: 1) trigger any enabled interrupt, 2) activate system reset or 3) cycle the power supply.
When the CPU has entered STOP mode there are only 2 ways to exit the mode: 1) activate system reset or 2) cycle the power supply.

The lowest possible power configuration is when disabling the flash, disabling the POR and shutting down both oscillators. In this case the

ZW0102 must be restarted by a system reset or a power cycle.

I/O Interfaces

The **ZW0102** has 11 configurable digital General Purpose I/O pins (GPIO pins). The GPIO pins are organized as three ports: *P0x* (4bits), *P2x* (3bits) and *P3x* (4bits). Some of the individual pins have dual functions – GPIO and a special HW function (for instance SPI interface, UART, TRIAC controller, etc.). All pins are CMOS compatible inputs/outputs.

There are four pins dedicated for general control of the chip: Power-On Reset Enable/Disable (*POR_E*), System Reset (*RESET_N*), Flash Programming Mode Select (*PROG_N*) and Production Test Mode Select (*TEST_N*).

Finally there are 13 analogue pins for RF interface, ADC, Bias Generator and crystal connections.

All GPIO pins will be set as inputs during reset. This pin configuration is maintained after the reset is released (until the SW changes the setting).

Pin Definitions

Table 1 gives the pin definitions of the **ZW0102**.

Table 1: ZW0102 – Pin Definitions

Pin Name(s)	# of Pins	Input / Output	Function
General Purpose I/O			
P00/SCK	1	I/O	User Programmable Pin / SPI interface - SCK (Clock signal)
P01/MOSI	1	I/O	User Programmable Pin / SPI interface - MOSI (Master Out Slave In)[3]
P02/MISO	1	I/O	User Programmable Pin / SPI interface - MISO (Master In Slave Out)[3]
P03	1	I/O	User Programmable Pin
P22/ZEROX	1	I/O	User Programmable Pin / ZEROX, Zero Crossing Detection Input for TRIAC Controller. The input buffer is an Schmitt Trigger for noise rejection.
P23/TRIAC	1	I/O	User Programmable pin / TRIAC. Output of Triac Controller (fire signal). The pin has extra high drive capability / slew rate.
P24	1	I/O	User Programmable Pin
P30/RXD0	1	I/O	User Programmable Pin / UART RxD Receive Data
P31/TXD0	1	I/O	User Programmable Pin / UART TxD Transmit Data
P32/INT_N	1	I/O	User Programmable Pin / External Interrupt Input (level-triggered or falling edge)
P34/PWM2	1	I/O	User Programmable Pin / PWM Output of Timer
General Control			
POR_E	1	I	Enable / Disable of Power-On Reset / Brown-out Circuit (0 = disable, 1 = enable)
RESET_N	1	I	Active Low System Reset Input. Internal pull-up of ~50kΩ
PROG_N	1	I	Flash Programming Mode Select (0 = programming mode, 1 = normal operation)
TEST_N	1	I	Production Test Mode Select (0 = test mode, 1 = normal operation). Internal pull-up of ~50kΩ. Should be left floating or

[3] **ZW0102** is master except during flash programming.

Pin Name(s)	# of Pins	Input / Output	Function
			tied to *DVDD*.

Pin Name(s)	# of Pins	Input / Output	Function
RF Interface			
RF_OUT	1	O	RF output to antenna.
RF_IN	1	I	RF input from antenna (external AC-coupling)
L[2:1]	2	NA	VCO. An external VCO inductor must be placed between these pins. The inductor value determines the RF operating frequency range.
CHP_OUT	1	O	Charge Pump Out.
ADC Interface			
AD[2:1]	2	I	Multiplexed Inputs for ADC
Clock Inputs			
XOSC_Qx	2	NA	Quartz Crystal Input for Primary Clock
XOSC32_Qx	2	NA	Quartz Crystal Input for Real Time Clock
Supply & Bias			
RBIAS	1	NA	Connection for external precision bias resistor (82kΩ, ±1%)
DVDD	4	NA	Positive Supply Digital Part
DGND_DSUB	2	NA	Negative Supply for Noise Shielding
DGND_SUP	5	NA	Negative Supply for Digital Supply
AVDD_VCO	1	NA	Positive Supply for VCO and Prescaler
AVDD_COMB	1	NA	Positive Supply for Analogue Part
AVDD_LNA_PA	1	NA	Positive Supply for LNA and PA
AVDD_MIX_IF	1	NA	Positive Supply for Mixer and IF
AVDD_ADC	1	NA	Positive Supply for ADC
AGND_MIX_IF	1	NA	Negative Supply for Mixer and IF
AGND_LNA_PA	1	NA	Negative Supply for LNA and PA
AGND_Pax	2	NA	Negative Supply for PA
AGND_COMB	1	NA	Negative Supply for Analogue Part
AGND_BACKPLANE	1	NA	Negative Supply for Backplane
AGND_ASUB	1	NA	Analogue Substrate Connection (P+ Guard)
AGND_ADC	1	NA	Negative Supply for ADC
AGND_VCO_PRE	1	NA	Negative Supply for VCO and Prescaler

SYSTEM INTERFACE

Figure 5 shows a typical **ZW0102** application circuit. The digital GPIO ports are programmable and can be used as interface to the user application. The RTC clock may not be needed in all applications. An optional filter (e.g. a SAW filter or a passive band pass filter) may be implemented in order to improve performance.

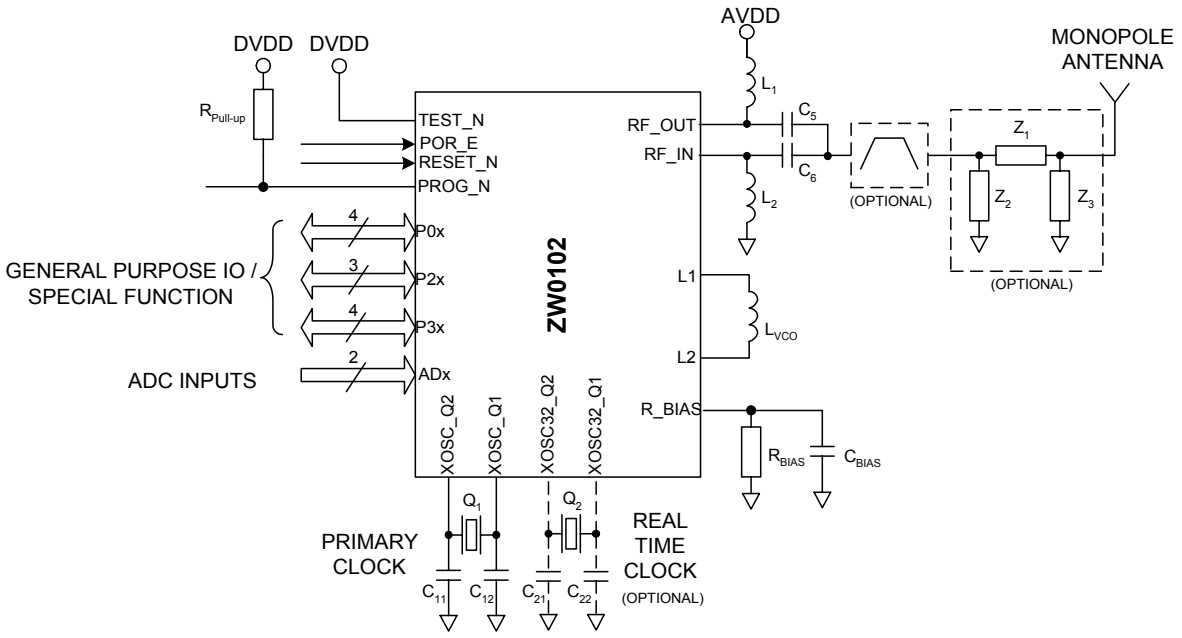


Figure 5: Typical ZW0102 Application Circuit

Clock Signals

The **ZW0102** includes an on-chip oscillator circuit for each clock input making it possible to drive crystals directly. The oscillators are designed for parallel mode operation of the crystals. Figure 6 shows the external crystal connections.

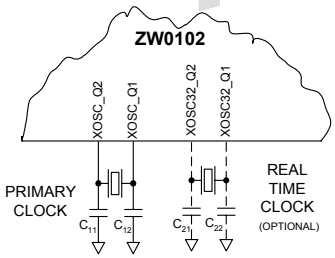


Figure 6: External Crystal Connections

An external load capacitor is required on each terminal of the crystals. The loading capacitor values depend on the total load capacitance, C_L, specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate at the specified frequency:

$$C_L := \frac{1}{\frac{1}{C_{x1}} + \frac{1}{C_{x2}}} + C_{paracitic} \quad ,$$

where the parasitic capacitance ($C_{paracitic}$) is constituted by the pin input capacitance and PCB stray capacitance. Typically the total parasitic capacitance is a few pF. The capacitors must refer to analog GND.

Reset

Figure 7 shows a simplified block diagram of the reset system.

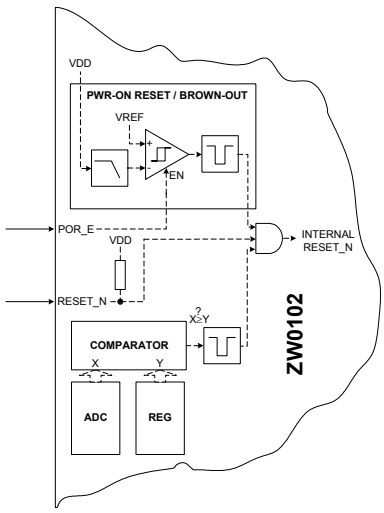


Figure 7: Reset Interface

An internal reset occurs when one or more of the following conditions are true:

1) *RESET_N* is low
2) When POR circuit detects low supply voltage
3) When ADC threshold is exceeded (ADC programmed to special mode)

The *RESET_N* is an asynchronous input. The signal is synchronized internally, so that the reset can be released independent of the timing of the active clock signal. If the primary crystal oscillator is inactive, the reset input should be held long enough for the oscillator to start up and stabilize (1024 clock periods of the primary clock)

The POR circuit contains a filter for glitch protection and hysteresis for noise and transient stability.

The POR and ADC reset signals will be held for 1024 clock periods of the primary clock after the signal is released. This will ensure a safe clock startup if the crystal oscillator was shut down. The duration of a watchdog reset is two clock periods of the system clock.

The POR circuit can be disabled by setting *POR_E* low. Disabling the POR will shut down the POR module in order to reduce power consumption.

During reset all GPIO pins will be configured as inputs and the RF will be powered down.

RF Transceiver

External Components

Figure 8 shows the RF interface in a typical application.

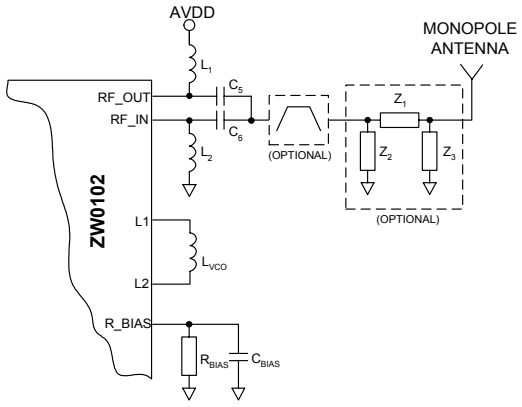


Figure 8: RF Interface in Typical Application

The RF transceiver requires very few external passive components for input/output matching and VCO.

L_2/C_6 is the input matching for the receiver. L_2 is also a DC choke for biasing. L_1/C_5 are used to match the transmitter to 50Ω. An internal T/R switch circuit makes it possible to connect the input and output together and match the **ZW0102** in both RX and TX mode. The typical values of the matching components are given in Table 2.

The purpose of Z_1, Z_2 and Z_3 is filtering and antenna matching. The typical values are given in Table 2[4].

The only external component of the VCO is the inductor L_{VCO} for tuning the RF operating frequency range. The typical value for this component is given in Table 2. It is recommended to use a high Q, low tolerance inductor for best performance. Moreover the VCO inductor should be placed as close as possible to the **ZW0102** in order to achieve an acceptable low level of LO leakage. In some cases it may even be advantageous to place the VCO inductor on the opposite side of the PCB using the GND layer as an effective shield between the inductor and the remaining RF circuitry.

The R_{BIAS} (and C_{BIAS}) determines the bias current to the analogue circuitry. The typical values of these components are given in Table 2.

Table 2: Typical RF Component Values

Part	868.42 (EU) / 908.42 (US)
C_{BIAS}	4.7pF ± 0.25pF
C_5	4.7pF ± 0.25pF
C_6	10 pF, 5%
Z_1	47 pF, 5% [1)]
Z_2	Not used [1)]
Z_3	Not used [1)]
L_1	2.5 nH, 5% (e.g. Coilcraft)
L_2	120 nH, 5% (e.g. Coilcraft)
L_{VCO}	US: 3.3 nH, 5% (High Q, e.g. Coilcraft) EU: 4.7 nH, 5% (High Q, e.g. Coilcraft)
R_{BIAS}	82 kΩ, 1%

[4] Z_2 and Z_3 may only be needed in some applications for matching to antenna.

[1] Antenna matching option

Additional external components (e.g. a SAW-filter or a passive band pass filter) may be added in order to improve selectivity and thereby performance of the receiver.

Antenna Considerations

The **ZW0102** can be used together with various types of antennas. The most common antennas for short-range communication are monopole, helical and loop antennas.

Monopole antennas are resonant antennas with a length corresponding to one quarter of the electrical wavelength (λ/4). They are very easy to design and can be implemented simply as a "piece of wire" or even integrated as a trace on the PCB.

Monopole antennas shorter than λ/4 can also be used, but at the expense of range. In size and cost critical applications such an antenna may very well be integrated into the PCB.

Helical antennas can be thought of as a combination of a monopole and a loop antenna. They are a good compromise in size critical applications. But helical antennas tend to be more difficult to optimise than the simple monopole.

Loop antennas are easy to integrate into the PCB, but are less effective due to difficult impedance matching because of their very low radiation resistance.

For low power applications the λ/4-monopole antenna is recommended giving the best range and because of its simplicity.

As a rule of thumb the λ/4 monopole antenna should be:

L = 7125 /f

Where f is in MHz, giving the length in cm. An antenna for 868.42 (EU) MHz should be 8.2 cm and an antenna for 908.42 (US) MHz should be 7.8 cm.

The antenna should be connected as close as possible to the **ZW0102**. The antenna should be matched to the feeding transmission line (50Ω).

RF Layout Considerations

The PCB wires in the RF layout should be as short as possible to avoid stray inductance. The wires should be routed over the analogue GND layer in order to provide a good transmission line and well determined characteristic impedance. Vias should be avoided in routing of signals. Preferably the RF components should be SMD components and the RF section should be kept isolated from surrounding circuitry.

*NOTE: Proper decoupling of the RF is absolutely paramount to the performance of the **ZW0102**. Please refer to the Decoupling section for this topic.*

UART

The **ZW0102** can control an UART (Universal Asynchronous Receiver Transmitter) interface with a data rate of 2.4kbps to 115kbps. The interface operates with 8 bit words, one start bit, one stop bit and no parity.

The interface is situated on *P30/RxD* and *P31/TxD*. Figure 9 shows a typical RS232 UART application circuit.

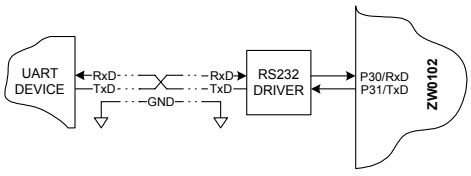


Figure 9: UART Interface in Typical Application

The UART shifts data in/out in the following order: start bit, data bits (LSB first) and stop bit. Figure 10 gives the waveform of a serial byte.

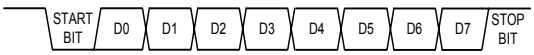


Figure 10: UART Waveform

Reception

For noise rejection, the serial port establishes the content of each received bit by a majority decision of 3 consecutive samples in the middle of each bit time. This is especially true for the start bit. If the falling edge on RxD is not verified by a majority decision of 3 consecutives samples (low), then the serial port stops

reception and waits for another falling edge on RxD.

After the middle of the stop bit time, the serial port waits for another high-to-low transition (start bit) on the RxD pin.

External Interrupt

The **ZW0102** supports one external interrupt on pin *P32/INT0_N*. The interrupt can be programmed to be either level-triggered (active low) or to be edge-triggered on falling edge.

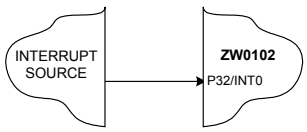


Figure 11: External Interrupt

Triac Controller

The **ZW0102** has a Triac Controller using phase control for power regulation of a resistive load. It has one input, *ZEROX* (Zero Crossing Detection), and one output *TRIAC* (triac fire pulse).

The phase control method conducts power during a specific time period in each half of the AC power cycle. A triac is commonly used to switch on/off the power to the load in the AC power system application. A gate voltage is required to turn on the triac (fire pulse). Once “on”, the triac will stay “on” until the AC sine wave approaches zero current regardless of the gate voltage. The power regulation is performed by simply controlling the fire angle (turn on start time). The triac will deliver the power to the load after the fire angle and turn off at the zero-crossing point.

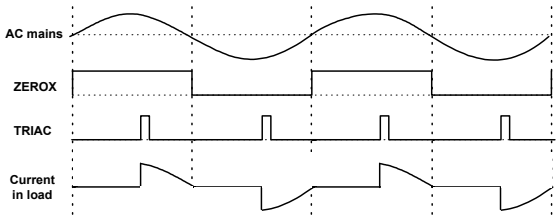


Figure 12: Triac Waveforms

Switching on the triac may produce noise on the AC mains. In case this noise is strong enough it could worst case cause additional triggering on the *ZEROX* as shown on Figure 13.

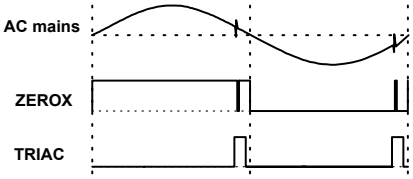


Figure 13: Triac Noise

In order to avoid these extra zero crossing triggers a noise mask has been implemented in the chip. The mask masks out zero crossings in a given period after the rising edge of *TRIAC* in order to circumvent this problem. Moreover it is necessary to apply a fire pulse of a certain duration in order to 1) provide sufficient charge for the triac to turn on and 2) to ensure that is does not subsequently switch off due to the potential noise. Both the duration of the mask and the fire pulse can be programmed in SW.

The triac controller is situated on the following pins *P22/ZEROX* and *P23/TRIAC*. The *P22/ZEROX* input is a Schmitt trigger input to avoid ringing on zero cross detection. The *P23/TRIAC* is a power output with extra high drive capability (8mA). Figure 14 shows a simplified application circuit.

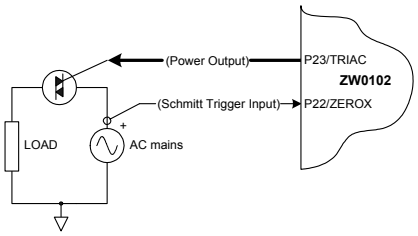


Figure 14: Simplified Triac Control Application

ADC

Figure 15 gives a block diagram of the **ZW0102** ADC function.

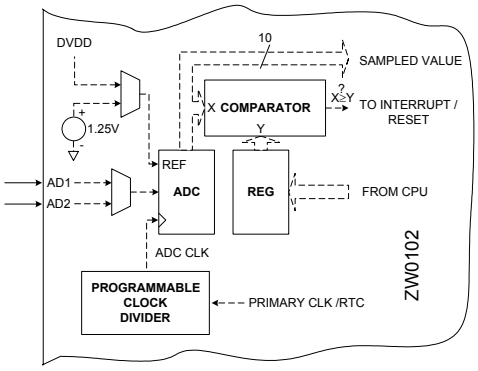


Figure 15: ADC Architecture

The ADC has a 10-bit resolution and can be programmed to refer to either VDD or an internal 1.25V bandgab reference. The input range is 0V to VDD where full scale (3FF hex) corresponds to the selected reference.

The ADC has two multiplexed analogue inputs: *AD1* and *AD2*.

The ADC function also includes a digital comparator function that compares the sampled value to a programmable threshold. The comparator can be programmed to generate an interrupt or a reset pulse when the value exceeds (or equals) the threshold. The ADC function is independent of the CPU. Thus the ADC can be programmed to wake up the processor from a STOP mode.

The sampling frequency is set by adjusting the division of the system clock. The maximum sampling frequency is 20.96 kHz. Each ADC conversion takes 11 ADC clock cycles regardless of the ADC clock frequency.

Serial Peripheral Interface - SPI

The Serial Peripheral Interface (SPI) allows synchronous data transfer between the **ZW0102** and peripheral devices or between a programming unit and the **ZW0102**. *Note: The SPI is not available for customer application in some Z-Wave API libraries.*

The **ZW0102** is master during normal operation and slave during programming mode. The programming mode is enabled by setting *PROG_N* low.

The interface consists of the pins *P00/SCK*, *P01/MOSI* and *P02/MISO*.

The *SCK* is the clock output in master mode and is the clock input in slave mode. During data transmission the SCK clocks the data from a 8-bit slave register into an 8-bit master register using the MISO connection (Master In Slave Out). At the same time data is clocked in the opposite direction from master to the slave using the MOSI (Master Out Slave In) connection. Consequently the two registers can be considered as one distributed 16-bit circular shift register. After 8 clock cycles the two registers will have swapped contents. The principle is illustrated in Figure 16.

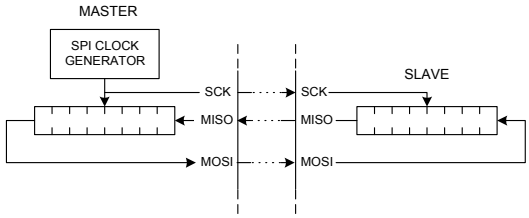


Figure 16: Data exchange between Master and Slave

In normal mode where the **ZW0102** is SPI master the sequencing of the data exchange can be programmed to be MSB first or LSB first. The output clocking of data can be programmed to be on rising edge or falling edge. The idle state of the SCK can be programmed to be high level or low level. The sampling of data will be on the opposite edge of output clocking. The two different clocking modes that can be programmed are shown on Figure 17.

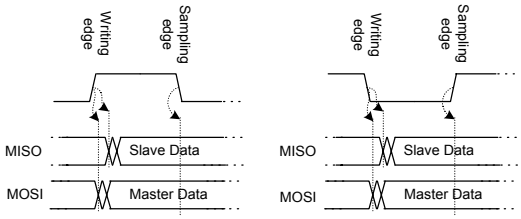


Figure 17: Clocking Modes

The SPI clock rate can be programmed to be $f_{sys}/8$, $f_{sys}/16$, $f_{sys}/32$ or $f_{sys}/64$ where f_{sys} is the system clock.

Figure 18 shows a typical application where the **ZW0102** operates as a master (normal mode). The CS (chip select) of the slave may be controlled by any available port on the **ZW0102.**

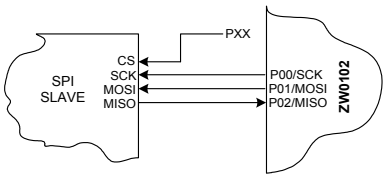


Figure 18: Typical Interface to Slave

External Programming of Flash

During flash programming (*PROG_N* low) an external master must control of the SPI bus. The SPI will automatically be set up for: 1) SCK=0 in idle and 2) data sampling on rising edge, data writing on falling edge. The watchdog function will be disabled as long as the *PROG_N* is low and all programmable ports will be tri-stated. Figure 19 gives a simplified block diagram of a typical interface to programming equipment.

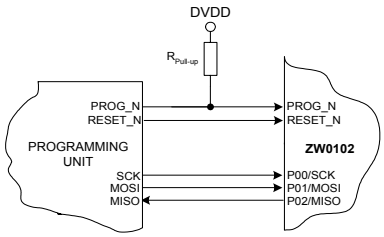


Figure 19: Interface to Programming Equipment

A dedicated instruction set is provided for controlling the **ZW0102** in programming mode. Using this instruction set it is possible to enable programming, erase the entire flash, read/write to flash, enable/disable read/write protection, set programming cycle time and read a signature byte. The instruction set is given in Table 3.

Table 3 Serial Programming Instruction Set

Instruction	Instruction Format Byte 1 MSB……LSB	Byte 2 MSB……LSB	Byte 3 MSB……LSB	Byte 4 MSB……LSB	Operation
Programming Enable	10101100	01010011	xxxxxxxx	xxxxxxxx	Enable serial interface for communication
Chip Erase	10101100	100xxxxx	xxxxxxxx	xxxxxxxx	Clears all pages (including lock bits)
Read Program Memory	0010h000	aaaaaaaa	bbbbbbxx	Oooooooo	Read high or low (h=1/h=0) byte o..o at address a..a:b..b:h
Set Write Cycle Time	10101100	01011101	xxxxxxxx	xxccccccc	Select number of clock cycles for flash programming time. (Further explanation given below)
Load Program Memory Page	0100h000	xxxxxxxx	bbbbbbxx	iiiiiiii	Write byte i..i to Program Memory page at address b..b:h
Write Program Memory Page	01001100	aaaaaaaa	xxxxxxxx	xxxxxxxx	Write page at address a..a
Write Lock Bits	10101100	111xxxxx	xxxxxxxx	000ppppp	Write lock bits p..p ‘1’ = unlocked. ‘0’ = locked
Read Lock Bits	01011000	xxxxxxxx	xxxxxxxx	xxxppppp	Read lock bits p..p ‘1’ = unlocked. ‘0’ = locked
Read Signature Byte	00110000	xxxxxxxx	xxxxxsss	oooooooo	Read signature byte o..o at address s..s

a: Page address, b: Even byte address, h: High or low (odd or even) byte, p: Lock Bits,
c: Clock timing bits, s: Signature byte address, i: Input data, o: Output data, x Don’t care

Each instruction is sent in the order bytes 1 to 4, most significant bits first (MSB). MSB is leftmost in all bit fields in the table. All 4 bytes must be sent, even if the last bits are 'x' - don't care. The individual instructions are further elaborated below.

Programming Enable

The 'Programming Enable' instruction enables the flash interface for communication. A flowchart for SPI communication is given in Figure 20. The chip must be powered-on and it must have a system clock running.

The synchronisation has taken place when the **ZW0102** echoes the second byte of the programming enable instruction back. The synchronisation may take up to 32 attempts. (typically synchronisation happens within 1-2 attempts).

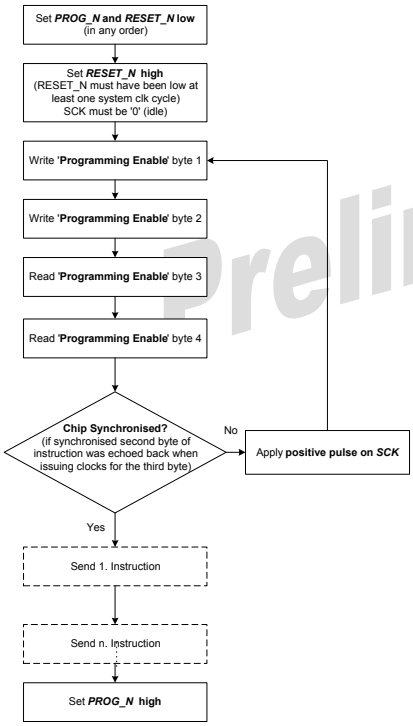


Figure 20: Enabling Flash Interface

Chip Erase

The 'Chip Erase' instruction restores the contents of all addresses to FF (hex) and can only by performed on the entire flash. The flash must be erased before programming.

The flash erase takes 225ms. Writing should not be performed until the flash erase is completed.

Read Program Memory

Reads a (high or low) byte at a given address in flash. [5]

Set Write Cycle Time

Before writing to the flash the write cycle time, t_{WC}, must be set in accordance with the device clock oscillator time. Using a system clock frequency of 7.376974 MHz it must be set to 001010 (binary).

Load Memory Page

Writing to the flash is performed in the following manner: 1) Write each byte that should be updated to a buffer (128 bytes located in SRAM) using the instruction 'Load Memory Page'. 2) Transfer the buffer to the flash using the instruction 'Write Program Memory Page'.

The programming sequence for one flash page is depicted in Figure 21.

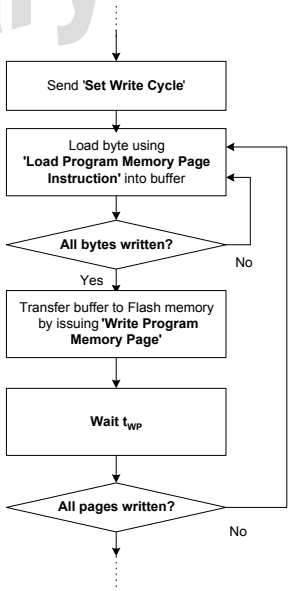


Figure 21: Programming Flash Pages

[5] When a read operation is performed it will take up to nine clock cycles before valid data are available on the SPI data output. The master must wait at least so many clock cycles before sending the first positive edge on SCK after the last negative edge of SCK for byte 3.

Please note that it is the whole buffer that is transferred from the SRAM. The bytes that have not been written by 'Load Program Memory Page' may assume random values from the SRAM.

Write Program Memory Page

The 'Write Program Memory Page' instruction transfers the content of a 128-byte buffer in SRAM to a page in flash (refer to the description of the 'Load Memory Page'). The writing operation (t_{WP}) takes 2.7ms.

Write Lock Bits

The function of the 'Write Lock Bits' instruction is threefold:

1) To enable read-back protection of the (entire) flash by clearing a dedicated bit, SPIRE (SPI Read Enable).

2) To enable protection of page 0 against inadvertent writing by clearing a dedicated bit, BOBLOCK (Boot Block Lock).

3) To define a boot sector that is secured against inadvertent writing. The size of the boot sector is programmable using 3 dedicated bits, BSIZE (Boot Sector Size). The boot block is from 7FFFF (hex) and downwards.

Figure 22 gives an overview of the flash protection.

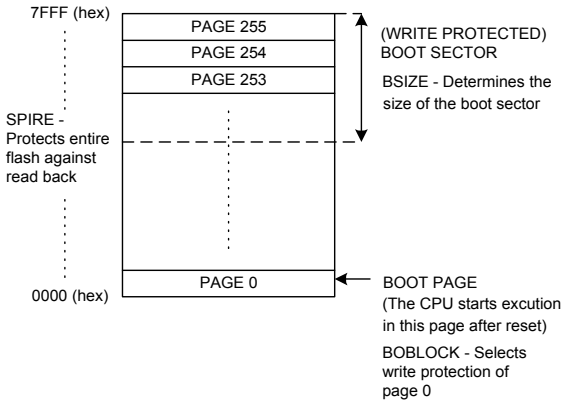


Figure 22: Overview of Flash Protection

Neither CPU nor SPI can write to the boot sector. The boot sector size is programmable in eight steps, from 0 to 32768 bytes through BSIZE. When the boot sector is selected to 32768 all available flash is allocated and the CPU and the SPI is prevented from writing to the flash memory.

Table 4 gives the coding of the individual flash memory lock bits

Table 4: Flash Memory Lock Bits

Bit	Name	Function
7:5	-	Reserved, write as '0'
4	BOBLOCK	Boot Block Lock 0: Page 0 is write protected 1: Page 0 is writeable, unless BSIZE = 000
3:1	BSIZE	Boot Sector Size 000: 32768 bytes (all) 001: 16384 bytes 010: 8192 bytes 011: 4096 bytes 100: 2048 bytes 101: 1024 bytes 110: 512 bytes 111: 0 bytes
0	SPIRE	SPI Read Flash Enable 0: SPI interface is not allowed to read flash data 1: SPI interface is allowed to read flash data

All locks are deactivated (set to 1) when the flash is erased using the 'Chip Erase' instruction. If multiple 'Write Lock Bits' instructions are issued without chip erase between, each lock bit will be AND'ed together with the previously written lock bits. In effect, this means that it is not possible to unlock the flash memory without also erasing it.

The lock bits can only be read through the SPI and not from the 8051 core.

The 'Write Lock Bits' takes 75us.

Read Lock Bits

The 'Read Lock Bits' instruction reads the status of the lock bits. Please refer to 'Write Lock Bits' for a further description.[6]

Read Signature Byte

The 'Read Signature Byte' instruction reads a signature byte from the chip. For the **ZW0102** there are 6 signature bytes. The sequence is: 7F-7F-7F-9E-95-05 (hex). [6].

Decoupling and Supply Considerations

A good decoupling strategy is absolutely paramount to achieve the best performance of the **ZW0102**. Bad decoupling may deteriorate the RF, increase LO leakage beyond regulatory limit, produce significant noise transients on V_{DD}, GND and I/O ports etc.

The decoupling of the supply should be placed as close as possible to the supply pins with minimum stray inductance. A decoupling capacitor should be provided for each supply pin. In some cases a pair of decoupling capacitors may be needed; one of them low valued (with minimum ESR) and one higher valued. Best performance of the decoupling is achieved if the via is placed on the opposite side of the decoupling capacitor with respect to the **ZW0102** as shown on Figure 23.

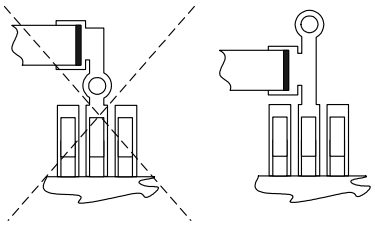


Figure 23: Optimal Placement of Via

When using the high drive capability of the triac controller extra attention is needed on power routing and decoupling in order to avoid noise on the supply (which could decrease the performance of the RF.)

For the *DVDD* (Digital supply) pins a typical decoupling value is 100nF for each supply pin. However for the analogue decoupling there are a few more considerations as discussed below.

It is recommended to use pairs of capacitors for the analogue RF pins. The capacitors should be positioned with the capacitor with lowest ESR closest to the chip. The capacitors should be placed between the dedicated supply pin and ground pin for each analogue function. The traces should always be extra wide.

During PCB layout the VCO inductor should be placed as close to the VCO pins as possible. The next priority should be to place the decoupling capacitors as close as possible to the pins *AVDD_VCO* and *AGND_VCO_PRE*.

SMD components with low ESR are preferable for decoupling.

The *AVDD* and the *DVDD* supply planes should be heavily decoupled and connected through a starpoint in order to avoid coupling of noise between the supplies. The analogue and digital ground can be coupled together in an internal ground layer.

Connecting Unused Inputs

Unused digital inputs should be tied to V_{DD} or GND to prevent the input from floating. If left to float, the power consumption of the device increases.

[6] When a read operation is performed it will take up to nine clock cycles before valid data are available on the SPI data output. The master must wait at least so many clock cycles before sending the first positive edge on SCK after the last negative edge of SCK for byte 3.

ZW0102 - SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [1)]

T_{OP}	Operating temperature[2)]	-40 °C to 125 °C
T_{STG1}	Storage Temperature (unprogrammed devices)	-40 °C to 150 °C
T_{STG2}	Storage Temperature (programmed devices)[2)]	-40 °C to 125 °C
T_{LEAD}	Lead Temperature (10 sec)	260 °C
$P_{RF,i}$	Input RF level..	10 dBm
V_{DD}	Supply voltage	-0.3 V to 5 V
V_I	Voltage on input pins	-0.3 V to V_{DD} + 0.3 V (5V max)

[1)] Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operations sections of this specification is not implied. Exposure to maximum ratings conditions for extended periods may affect device reliability.
[2)] Data retention for a programmed device is better than 0.49 years at 125°C

***Caution!** ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

RECOMMENDED OPERATION CONDITIONS

Parameter		Min	Nom	Max	Unit
T_{OP}	Operating temperature	-35		85	°C
V_{DD}	Supply voltage	2.7		3.6	V
f_{pri}	Primary Clock crystal frequency		7.376974		MHz
f_{RTC}	RTC frequency		32.768		kHz

ELECTRICAL CHARACTERISTICS

Supply Current / Power Consumption (T_A=25 °C, V_{DD} =3.3V unless otherwise specified)

Parameter		Condition	Min	Typ	Max	Unit
I_{VDD}	Supply current	@Lowest Power - Scenario 1 [1)]		0.15		µA
		@Timer wake up – Scenario 2 [2)]		30		µA
		@Simple program – Scenario 3 [3)]		9.6		mA
		@Receive mode – Scenario 4 [4)]		21		mA
		@Transmit max – Scenario 5 [5)]		35		mA
		@Transmit -5dBm – Scenario 6 [6)]		25		mA
MODULES IN ON/OFF [7)]						
I_{ADC}	ADC supply current	@System running on RTC		165		µA
I_{POR}	POR supply current			35		µA
$I_{FL\ ON}$	Flash on supply current			2.9		mA
$I_{FL\ DI}$	Flash disabled between instructions supply current			1.5		mA
I_{RTC}	RTC supply current			2.5		µA
I_{CLK}	Main clk supply current			252		µA

NOTES
[1)] Also denoted: STOP-Mode. Lowest possible power configuration. Both clocks are powered down. The ADC and the POR

modules are disabled. The RF transceiver is off. The flash is shut down. An external reset pulse or a power cycle must be provided to restart the device.

[2] Also denoted: Sleep Mode + RTC. Periodically wake-up configuration with the CPU in Idle condition and the flash is disabled between instructions. A timer is used to wake up the device every 20 seconds (by asserting an interrupt). The chip runs on the RTC clock. The stated current is the steady state current consumption between interrupts. The ADC and the POR modules are disabled. The RF transceiver is off.

[3] Simple program execution configuration. The CPU is running a simple 'While 1;'-loop using the 7.376974 MHz system clock. The ADC and the POR modules are disabled. The RF transceiver is off. The flash is disabled between instructions.

[4] Receive Mode. The RF transceiver is set in receive mode. The CPU is running a simple 'While 1;'-loop. The ADC and POR are disabled. The flash is on.

[5] Transmission Mode with maximum output power. The microcontroller is running a simple 'While 1;'-loop. The ADC and POR are disabled. The flash is on.

[6] Transmission Mode with –5dBm output power measured on a Z-Wave Module PCB (refer to footnote [7]). The microcontroller is running a simple 'While 1;'-loop. The ADC and POR are disabled. The flash is on.

[7] Current consumption of sub-circuits that can be shut down or set in power saving mode.

Power Consumption vs. Transmission Power

The Figure 24 shows the typical power consumption vs. transmission power. The measurement was performed on a Z-Wave Module.[7]

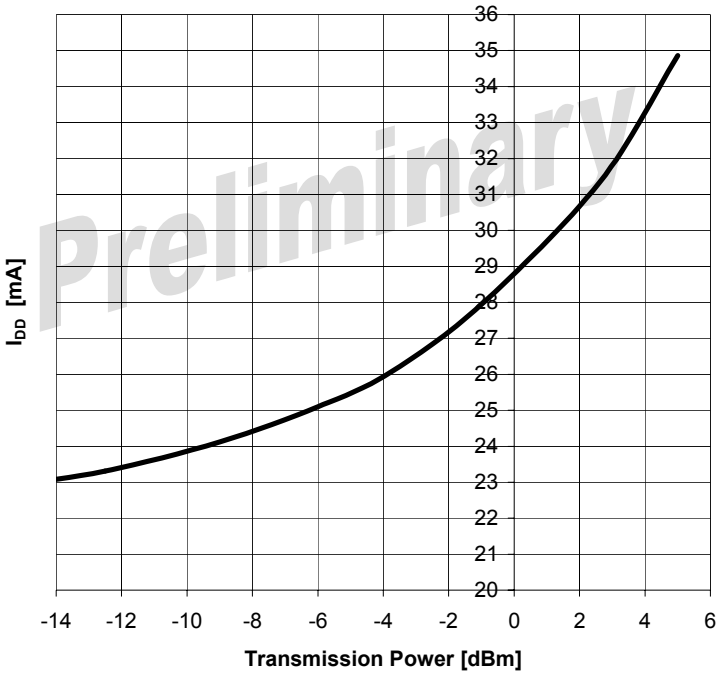


Figure 24: Power Consumption vs. Transmission Power (T_A=25 °C, V_{DD}=3.3V)

[7] The Z-Wave Module is a PCB developed by Zensys that implements the typical application as stated on Figure 5.

ELECTRICAL CHARACTERISTICS

DC Characteristics (T_A=25 °C, V_{DD}=3.3V unless otherwise specified)

Parameter	Condition	Min	Typ	Max	Unit
POWER-ON-RESET (POR)					
V_{th} Threshold		2.7	2.9	3.1	V
V_h Hysteresis			30		mV
PRIMARY CLOCK OSCILLATOR					
T_{total} Total Crystal Tolerance [1]				±25	ppm
DIGITAL INPUTS					
RESET_N, TEST_EN_N [2]					
V_{IH} High-level Input Voltage		0.7·V_{DD}			V
V_{IL} Low-level Input Voltage				0.3·V_{DD}	V
I_{IH} High-level Input Current	@ V_{IH}=V_{DD}			1	µA
I_{IL} Low-level Input Current	@ V_{IL}=0V		-52		µA
POR_E, PROG_N, Pxy except P22					
V_{IH} High-level Input Voltage		0.7·V_{DD}			V
V_{IL} Low-level Input Voltage				0.3·V_{DD}	V
I_{IH} High-level Input Current	@ V_{IH}=V_{DD}			1	µA
I_{IL} Low-level Input Current	@ V_{IL}=0V			-1	µA
P22/ZEROX [3]					
V_{T+} Positive-going Threshold			2.0		V
V_{T-} Negative-going Threshold			1.1		V
V_H Hysteresis Voltage (V_{T+}-V_{T-})			1.0		V
I_{IH} High-level Input Current	@ V_{IH}=V_{DD}			1	µA
I_{IL} Low-level Input Current	@ V_{IL}=0V			-1	µA
DIGITAL OUTPUTS					
Pxy except P23/TRIAC					
V_{OH} High-level Output Voltage	@ I_{OH}=2mA		3.1		V
V_{OL} Low-level Output Voltage	@ I_{OL}=-2mA		0.2		V
P23/TRIAC [4]					
V_{OH} High-level Output Voltage	@ I_{OH}=8mA		3.0		V
V_{OL} Low-level Output Voltage	@ I_{OL}=-8mA		0.2		V
DIGITAL INPUTS					
C_I Input capacitance			8		pF
ADC INPUTS					
AD1, AD2					
Z_I Input Impedance			>300		MΩ
V_I Input Voltage Range		0		V_{DD}	V
E_{fs} Full scale error			±2		LSB
V_{ref} Internal Reference Accuracy			±1		%

NOTES

[1] The crystal frequency tolerance (initial tolerance, ageing, temperature dependency, etc.) will determine the frequency accuracy of the transmitted signal and will influence the receivers frequency lock range.

[2] Inputs with internal pull-up of approximately 50kΩ.

[3] Schmitt Trigger input

[4] Power / high slew rate output

Output Characteristic

The **ZW0102** GPIO's are slew rate limited and have a typical drive capability as indicated on Figure 25.

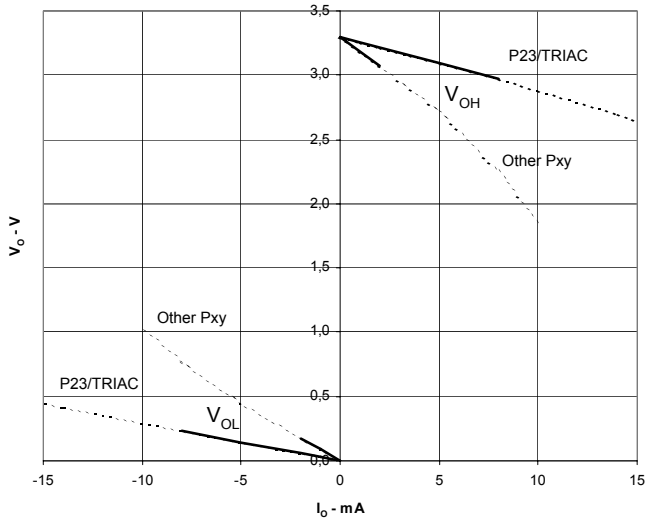


Figure 25: Typical Output Characteristic (T_A=25 °C, V_{DD}=3.3V)

ELECTRICAL CHARACTERISTICS

AC Characteristics (C_L=50pF, T_A=25 °C, V_{DD}=3.3V unless otherwise specified)

Parameter	Condition	Min	Typ	Max	Unit
POWER-ON-RESET (POR)					
G Glitch immunity[1)]		250	1000	2000	nVs
RISE/FALL TIME					
Pxy except P23/TRIAC					
t_r Rise Time			17		ns
t_f Fall Time			15		ns
P23/TRIAC [2)]					
t_r Rise Time			7		ns
t_f Fall Time			5		ns

NOTES

[1)] Glitch immunity: Maximum transient duration multiplied by comparator overdrive without causing a reset pulse (i.e.: 1000 nVs glitch immunity ⇒ a 10 μs transient of 100 mV below threshold will not cause a reset pulse)

[2)] Power / high slew rate output

Capacitive Loading

Figure 26 shows the typical capacitive loading characteristic for the **ZW0102**

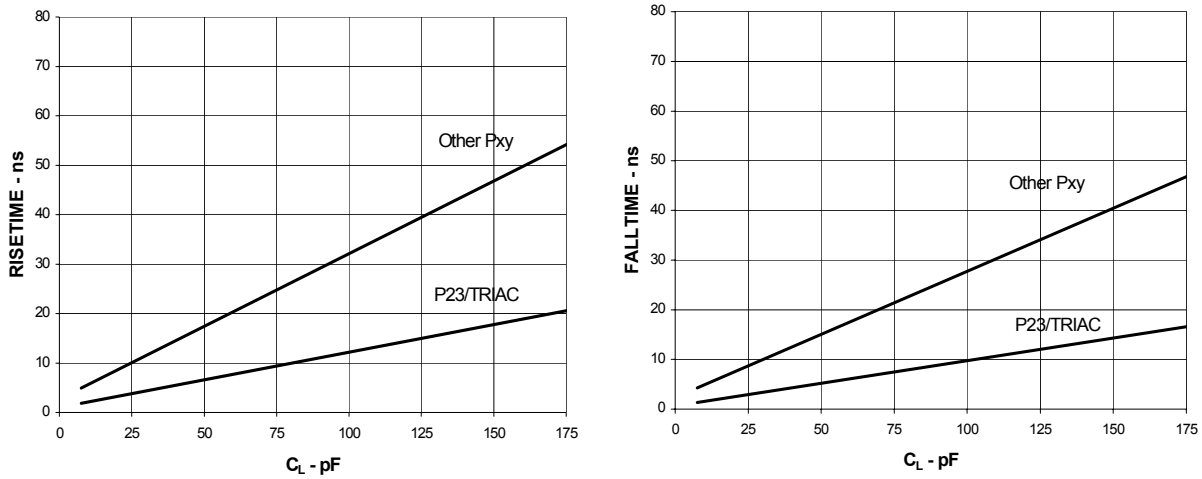


Figure 26: Typical Rise / Fall Time (TA=25 °C)

ELECTRICAL CHARACTERISTICS

RF Characteristics (T_A=25 °C, V_{DD}=3.3V unless otherwise specified)

Parameter		Condition	Min	Typ	Max	Unit
TRANSMIT						
$P_{RF,oMx}$	Max Output Power	@50Ω load		5		dBm
$P_{RF,oMn}$	Min Output Power	@50Ω load		-29		dBm
$Z_{RF,o}$	RF Output Impedance	@900MHz		7-j12		Ω
P_h	Harmonics[1)]			-18		dBc
RECEIVE						
$P_{RF,s}$	Receiver Sensitivity [2)]			-98		dBm
$P_{RF,L}$	LO Leakage				-57	dBm
$Z_{RF,i}$	RF Input Impedance	@908 MHz		45Ω / 0.4nH		Ω, nH
FREQUENCY SYNTHESISER						
N_p	Output signal phase noise	100kHz offset from carrier		-85		dBc /Hz

NOTES
1) An external LC or SAW filter should be used to reduce harmonics emission to comply with SRD requirements.
2) Measured on 19.2kbaud manchester encoded Z-wave frames (datarate = 9.6kbits/s). FER (frame error rate) better than 10^{-2}.

TIMING PARAMETERS

(T_A=25 °C, V_{DD}=3.3V unless otherwise specified)

Parameter	Condition	Min	Typ	Max	Unit
POWER-ON-RESET (POR)					
t_P Reset active timeout period		200	330	500	µs
SYSTEM RESET (*RESET_N*)					
t_{reset} Input reset pulse		1024·f_{clk} [1]			
t_{resetR} Rise time	10% to 90%			400	µs
t_{resetF} Fall time	90% to 10%			400	µs
PRIMARY CLOCK OSCILLATOR					
t_{SON} Turn-on time				5	ms
RTC OSCILLATOR					
t_{RON} Turn-on time			160		ms
RF PART					
t_{PLLon} PLL turn-on time			250		µs
$t_{PLLturn}$ PLL lock time (RX/TX turn time)			200		µs
ADC					
f_s Sampling frequency				20.96	kHz
t_c Conversion Time		44		11·$f_{AD\ clk}$ [2]	µs
SPI FLASH PROGRAMMING					
f_{SCK} SCK frequency				f_{clk} / 8 [3]	
t_{Low} SCK low period		4·T_{clk} [3]			
t_{High} SCK high period		4·T_{clk} [3]			
t_{Rise} SCK Rise time	10% to 90%			T_{clk} / 2 [3]	ns
t_{Fall} SCK Fall time	90% to 10%			T_{clk} / 2 [3]	ns
t_{Setup} Data Setup Time		T_{clk} [3]			
t_{Hold} Data Hold Time		T_{clk} [3]			
t_{Data} Delay from SCK falling edge to valid data				T_{clk} [3]	
SPI INSTRUCTION TIMING					
t_{ER} Flash erase duration		225		450	ms
t_{ACC} Read operation access time				9·T_{clk} [3] [4]	
t_{WP} Write Page duration		2.7		5.4	ms
t_{WL} Write Lock Bits duration		75		150	µs

NOTES
[1] The reset input should be held long enough for the oscillator to start up and stabilize (1024 clock periods of the primary clock).
[2] $f_{AD\ clk}$ is the ADC clock. It can be programmed as a division of the primary clock or the RTC. The (sub-divided) ADC clock must repect a maximum clock frequency of 250kHz.
[3] f_{clk} is the system clock. T_{clk} is the period of the system clock (= 1/ f_{clk}).
[4] When a read operation is performed it will take up to nine clock cycles before valid data are available on the SPI data output. The master must wait at least so many clock cycles before sending the first positive edge on SCK after the last negative edge of SCK for byte 3.

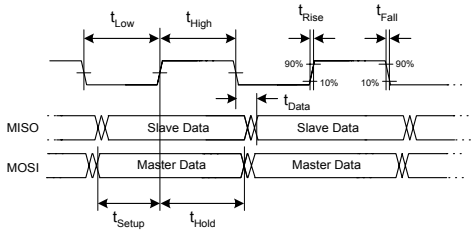
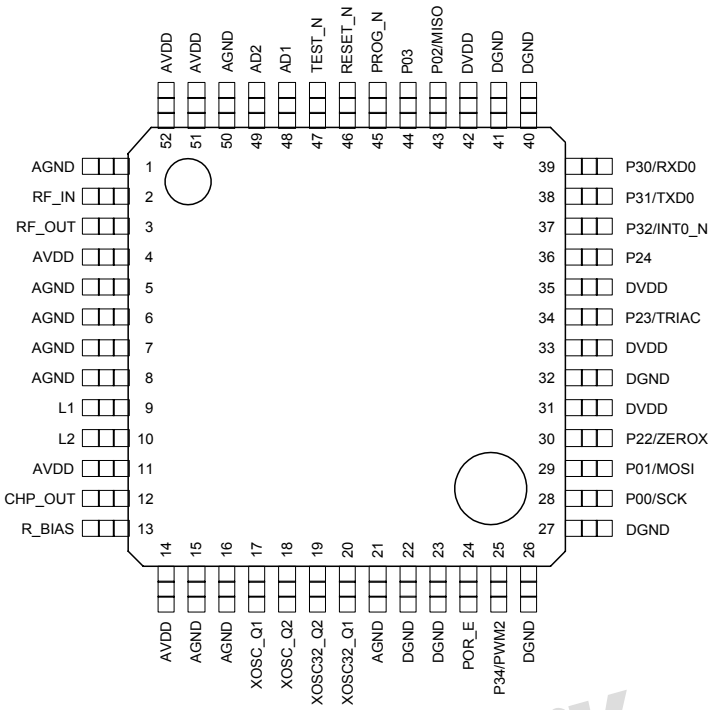


Figure 27: SPI Flash Programming Timing

PIN CONFIGURATION

(52 PINS TQFP, TOPVIEW)



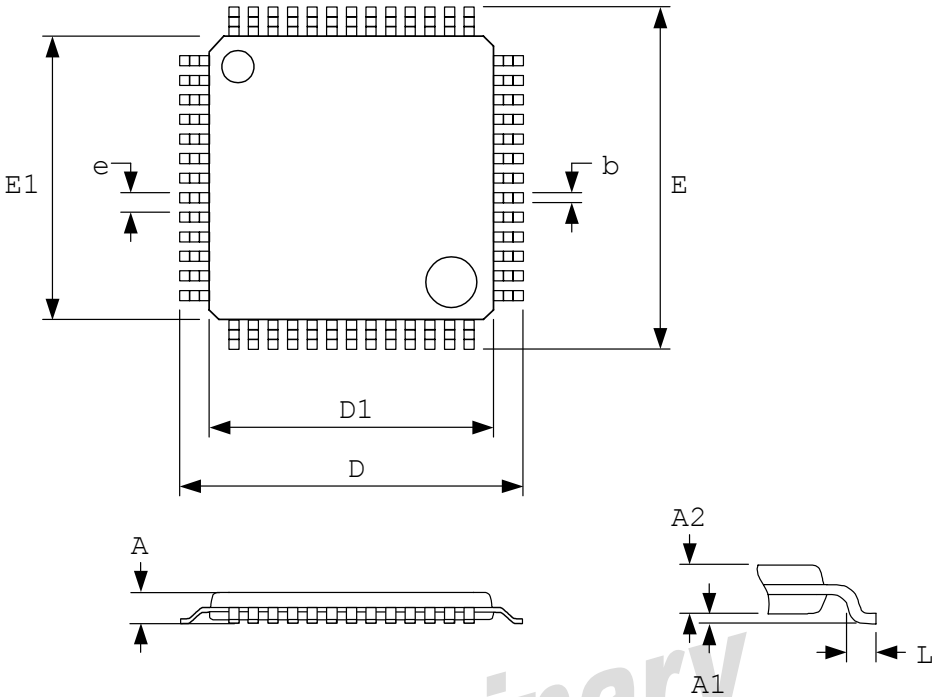
Pin	Pin Name	Pin Type
1	AGND Mixer	Power
2	RF_IN	RF input [1]
3	RF_OUT	RF output [1]
4	AVDD LNA/PA	Power
5	AGND LNA/PA	Power
6	AGND PA	Power
7	AGND PA	Power
8	AGND VCO/Presaler	Power
9	L1	RF[1]
10	L2	RF[1]
11	AVDD VCO/ Prescaler	Power
12	CHP_OUT	Analogue Output
13	R_BIAS	Analogue
14	AVDD	Power
15	AGND	Power
16	AGND	Power
17	XOSC_Q1	Analogue Input
18	XOSC_Q2	Analogue Output
19	XOSC32_Q2	Analogue Input
20	XOSC32_Q1	Analogue Output
21	AGND P+ guard	Power
22	DGND Noise shield	Power
23	DGND Noise shield	Power
24	POR_E	Digital Input
25	P34/PWM2	Digital Tristate I/O
26	DGND	Power

Pin	Pin Name	Pin Type
27	DGND	Power
28	P00/SCK	Digital Tristate I/O
29	P01/MOSI	Digital Tristate I/O
30	P22/ZEROX	Digital Tristate I/O [2]
31	DVDD	Power
32	DGND	Power
33	DVDD Noise shield	Power
34	P23/TRIAC	Digital Tristate I/O [3]
35	DVDD	Power
36	P24	Digital Tristate I/O
37	P32/INT0_N	Digital Tristate I/O
38	P31/TXD0	Digital Tristate I/O
39	P30/RXD0	Digital Tristate I/O
40	DGND	Power
41	DGND	Power
42	DVDD	Power
43	P02/MISO	Digital Tristate I/O
44	P03	Digital Tristate I/O
45	PROG_N	Digital Input
46	RESET_N	Digital Input
47	TEST_N	Digital Input
48	AD1	Analogue Input
49	AD2	Analogue Input
50	AGND ADC	Power
51	AVDD ADC	Power
52	AVDD Mixer/IF	Power

[1] No ESD diode protection
[2] Schmitt Trigger input
[3] Power / high slew rate output

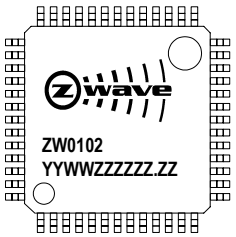
PACKAGE OUTLINE DIMENSIONS

(52 PINS TQFP, TOPVIEW)



Symbol	Min	Typ	Max	Unit	Remark
A			1.20	mm	Package height
A1	0.05		0.15	mm	
A2	0.95	1.00	1.05	mm	
D		12.0		mm	
D1		10.0		mm	
E		12.0		mm	
E1		10.0		mm	Body size
L	0.45	0.60	0.75	mm	
e		0.65		mm	Pin pitch
b	0.22	0.32	0.38	mm	

DEVICE MARKING



Marking	Meaning
YY	Year
WW	Week
ZZZZZZ.ZZ	Batch number